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WITH THE END OF DENNARD SCALING AND MOORE'S LAW IC CHIPS ESPECIALLY LARGE SCALE ONES NOW FACE MORE RELIABILITY CHALLENGES AND RELIABILITY HAS BECOME ONE OF THE MAINSTAY MERITS OF VLSI DESIGNS IN THIS CONTEXT THIS BOOK PRESENTS A BUILT-IN ON-CHIP FAULT-TOLERANT COMPUTING PARADIGM THAT SEEKS TO COMBINE FAULT DETECTION, FAULT DIAGNOSIS AND ERROR RECOVERY IN LARGE SCALE VLSI DESIGN IN A UNIFIED MANNER SO AS TO MINIMIZE RESOURCE OVERHEAD AND PERFORMANCE PENALTIES. FOLLOWING THIS COMPUTING PARADIGM WE PROPOSE A HOLISTIC SOLUTION BASED ON THREE KEY COMPONENTS: SELF-TEST, SELF-DIAGNOSIS AND SELF-REPAIR OR 3S. FOR SHORT WE THEN EXPLORE THE USE OF 3S FOR GENERAL IC DESIGNS, GENERAL PURPOSE PROCESSORS, NETWORK ON CHIP (NOC) AND DEEP LEARNING ACCELERATORS AND PRESENT PROTOTYPES TO DEMONSTRATE HOW 3S RESPONDS TO IN-FIELD SILICON DEGRADATION AND RECOVERY UNDER VARIOUS RUNTIME FAULTS CAUSED BY AGING, PROCESS VARIATIONS OR RADICAL PARTICLES. MOREOVER WE DEMONSTRATE THAT 3S NOT ONLY OFFERS A POWERFUL BACKBONE FOR VARIOUS ON-CHIP FAULT-TOLERANT DESIGNS AND IMPLEMENTATIONS BUT ALSO HAS FURTHER REACHING IMPLICATIONS SUCH AS MAINTAINING GRACEFUL PERFORMANCE DEGRADATION, MITIGATING THE IMPACT OF VERIFICATION BLIND SPOTS AND IMPROVING CHIP YIELD. THIS BOOK IS THE OUTCOME OF EXTENSIVE FAULT-TOLERANT COMPUTING RESEARCH PURSUED AT THE STATE KEY LAB OF PROCESSORS, INSTITUTE OF COMPUTING TECHNOLOGY, CHINESE ACADEMY OF SCIENCES OVER THE PAST DECADE. THE PROPOSED BUILT-IN ON-CHIP FAULT-TOLERANT COMPUTING PARADIGM HAS BEEN VERIFIED IN A BROAD RANGE OF SCENARIOS FROM SMALL PROCESSORS IN SATELLITE COMPUTERS TO LARGE PROCESSORS IN HPCS. HOPEFULLY IT WILL PROVIDE AN ALTERNATIVE YET EFFECTIVE SOLUTION TO THE GROWING RELIABILITY CHALLENGES FOR LARGE SCALE VLSI DESIGNS.

INHALTSANGABE

ABSTRACT

TWO EVOLUTIONARY APPROACHES OF ALLOCATING TASKS ONTO A FIELD PROGRAMMABLE GATE ARRAY (FPGA) ARE PRESENTED: OFFLINE TASK ARRANGEMENT (WHENEVER A SET OF TASKS HAS TO BE ARRANGED ONTO AN FPGA IN PRACTICE ONE IS INTERESTED IN ARRANGING A MAXIMUM NUMBER OF TASKS WHICH EFFICIENTLY UTILIZE THE FPGA AREA) AND ONLINE TASK ARRANGEMENT (FPGAS THAT ALLOW PARTIAL RECONFIGURATION AT RUN-TIME CAN BE SHARED AMONG MULTIPLE INDEPENDENT TASKS WHEN THE SEQUENCE OF TASKS TO BE PERFORMED IS UNPREDICTABLE THE FPGA CONTROLLER NEEDS TO MAKE ALLOCATION DECISIONS ONLINE SINCE ONLINE ALLOCATION SUFFERS FROM FRAGMENTATION TASKS CAN END UP WAITING DESPITE THERE BEING SUFFICIENT ALBEIT NON-CONTIGUOUS RESOURCES AVAILABLE TO SERVICE THEM THE TIME TO COMPLETE TASKS IS CONSEQUENTLY LONGER AND THE UTILIZATION OF THE FPGA IS LOWER THAN IT COULD BE). A GENETIC ALGORITHM IS PROPOSED REARRANGING A SUBSET OF THE TASKS EXECUTING ON THE FPGA WHEN DOING SO ALLOWS THE NEXT PENDING TASK TO BE PROCESSED SOONER IN COMPARISON WITH OTHER HEURISTIC APPROACHES. A GENETIC ALGORITHM IS DESCRIBED AND EVALUATED WHICH OVERCOMES THE NP-HARD PROBLEMS OF

USBF P P 202104-28 WITH THE END OF DENNARD SCALING AND MOORE'S LAW IC CHIPS ESPECIALLY LARGE SCALE ONES NOW FACE MORE RELIABILITY CHALLENGES AND RELIABILITY HAS BECOME ONE OF THE MAINSTAY MERITS OF VLSI DESIGNS IN THIS CONTEXT THIS BOOK PRESENTS A BUILT-IN ON-CHIP FAULT-TOLERANT COMPUTING PARADIGM THAT SEEKS TO COMBINE FAULT DETECTION, FAULT DIAGNOSIS AND ERROR RECOVERY IN LARGE SCALE VLSI DESIGN IN A UNIFIED MANNER SO AS TO MINIMIZE RESOURCE OVERHEAD AND PERFORMANCE PENALTIES FOLLOWING THIS COMPUTING PARADIGM WE PROPOSE A HOLISTIC SOLUTION BASED ON THREE KEY COMPONENTS: SELF-TEST, SELF-DIAGNOSIS AND SELF-REPAIR OR 3S FOR SHORT. WE THEN EXPLORE THE USE OF 3S FOR GENERAL IC DESIGNS, GENERAL PURPOSE PROCESSORS, NETWORK ON CHIP, NOC AND DEEP LEARNING ACCELERATORS AND PRESENT PROTOTYPES TO DEMONSTRATE HOW 3S RESPONDS TO IN-FIELD SILICON DEGRADATION AND RECOVERY UNDER VARIOUS RUNTIME FAULTS CAUSED BY AGING, PROCESS VARIATIONS OR RADICAL PARTICLES. MOREOVER WE DEMONSTRATE THAT 3S NOT ONLY OFFERS A POWERFUL BACKBONE FOR VARIOUS ON-CHIP FAULT-TOLERANT DESIGNS AND IMPLEMENTATIONS BUT ALSO HAS FURTHER REACHING IMPLICATIONS SUCH AS MAINTAINING GRACEFUL PERFORMANCE DEGRADATION, MITIGATING THE IMPACT OF VERIFICATION BLIND SPOTS AND IMPROVING CHIP YIELD. THIS BOOK IS THE OUTCOME OF EXTENSIVE FAULT-TOLERANT COMPUTING RESEARCH PURSUED AT THE STATE KEY LAB OF PROCESSORS, INSTITUTE OF COMPUTING TECHNOLOGY, CHINESE ACADEMY OF SCIENCES OVER THE PAST DECADE. THE PROPOSED BUILT-IN ON-CHIP FAULT-TOLERANT COMPUTING PARADIGM HAS BEEN VERIFIED IN A BROAD RANGE OF SCENARIOS FROM SMALL PROCESSORS IN SATELLITE COMPUTERS TO LARGE PROCESSORS IN HPCS. HOPEFULLY IT WILL PROVIDE AN ALTERNATIVE YET EFFECTIVE SOLUTION TO THE GROWING RELIABILITY CHALLENGES FOR LARGE SCALE VLSI DESIGNS.

BUILT-IN FAULT-TOLERANT COMPUTING PARADIGM FOR RESILIENT LARGE-SCALE CHIP DESIGN 2023-03-01 INHALTSANGABE ABSTRACT
TWO EVOLUTIONARY APPROACHES OF ALLOCATING TASKS ONTO A FIELD PROGRAMMABLE GATE ARRAY (FPGA) ARE PRESENTED: OFFLINE TASK ARRANGEMENT (WHENEVER A SET OF TASKS HAS TO BE ARRANGED ONTO AN FPGA IN PRACTICE ONE IS INTERESTED IN ARRANGING A MAXIMUM NUMBER OF TASKS WHICH EFFICIENTLY UTILIZE THE FPGA AREA) A GENETIC ALGORITHM IS PROPOSED SEARCHING FOR AN ARRANGEMENT OF TASKS OFFLINE I.E. BEFORE THE TASKS ARE PHYSICALLY PLACED ONTO THE FPGA. ONLINE TASK ARRANGEMENT (FPGAS THAT ALLOW PARTIAL RECONFIGURATION AT RUN TIME CAN BE SHARED AMONG MULTIPLE INDEPENDENT TASKS WHEN THE SEQUENCE OF TASKS TO BE PERFORMED IS UNPREDICTABLE THE FPGA CONTROLLER NEEDS TO MAKE ALLOCATION DECISIONS ONLINE SINCE ONLINE ALLOCATION SUFFERS FROM FRAGMENTATION TASKS CAN END UP WAITING DESPITE THERE BEING SUFFICIENT ALBEIT NON-CONTIGUOUS RESOURCES AVAILABLE TO SERVICE THEM THE TIME TO COMPLETE TASKS IS CONSEQUENTLY LONGER AND THE UTILIZATION OF THE FPGA IS LOWER THAN IT COULD BE) A GENETIC ALGORITHM IS PROPOSED REARRANGING A SUBSET OF THE TASKS EXECUTING ON THE FPGA WHEN DOING SO ALLOWS THE NEXT PENDING TASK TO BE PROCESSED SOONER IN COMPARISON WITH OTHER HEURISTIC APPROACHES. A GENETIC ALGORITHM IS DESCRIBED AND EVALUATED WHICH OVERCOMES THE NP-HARD PROBLEMS OF IDENTIFYING FEASIBLE REARRANGEMENTS AND SCHEDULING THE REARRANGEMENTS WHEN MOVING TASKS ARE RELOADED FROM OFF-CHIP.
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