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global signals for activating the word lines passing and latching the address set up time hold time enabling and disabling pre charge read select timing and write select timing an sram static random access memory is designed to fill two needs to provide a direct interface with the cpu at speeds not attainable by drams and to replace drams in systems that require very low power consumption how is sram different from dram in terms of circuit design sram and dram differ in their basic cell structure sram cells use flip flops typically composed of multiple transistors while dram cells use capacitors and require refreshing circuits sram schematic diagrams are essential tools for understanding and designing static random access memory sram circuits these diagrams provide a visual representation of the circuit s components and their interconnections high performance and low power sram cell design using power gating technique in this paper the stable and power efficient method is presented to design and implement static ram cell static ram is one of the essential building block for the vlsi design an ofet sram is developed to hide the slow transition of the actuators developed five transistor sram cell reduces the number of the bit lines by one half and reduces the sram cell area by 20 pipelining the write operation reduced the sram write time by 69 simulations show that two dimensional material based static random access memory sram circuits leverage their low parasitic capacitance counteracting performance declines due to increased

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